MICRO-331 Microfabrication technologies

Lithography

2024 edition

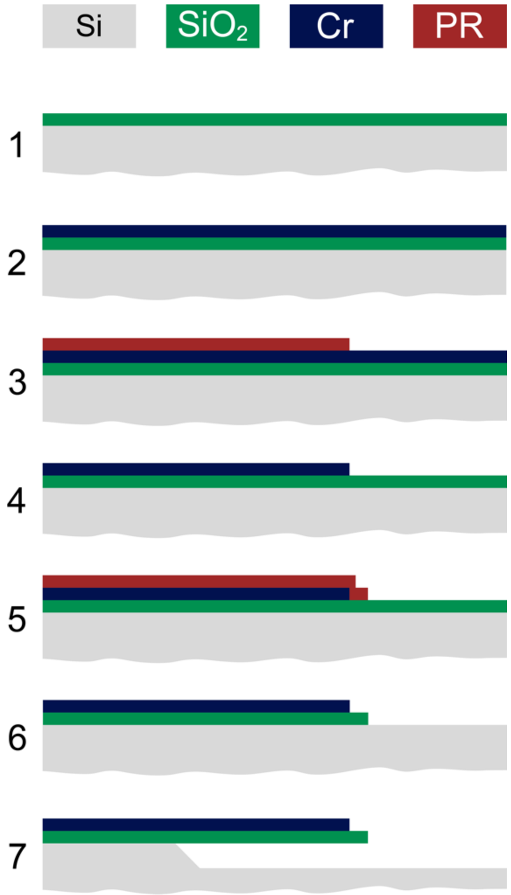
Today - Lithography

Key aspects to remember
- Resists
- Writer and projection/mask
- Resolution and throughput
- Lift-off

Industry standard today

Alternative lithography
- Stencil
- Nanoimprint
- microcontact printing
- scanning nanoprobes

2 lithography steps for the bimorph device



Oxidation

Cr layer deposition

Lithography 1 (heater)

Cr etch

Lithography 2 (cantilever)

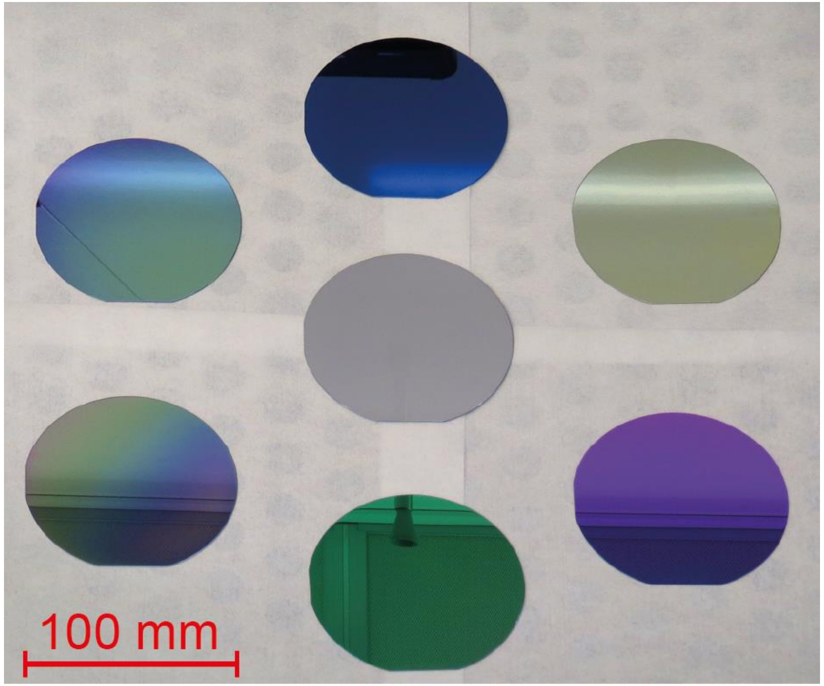
+ alignment

SiO2 etch in BHF

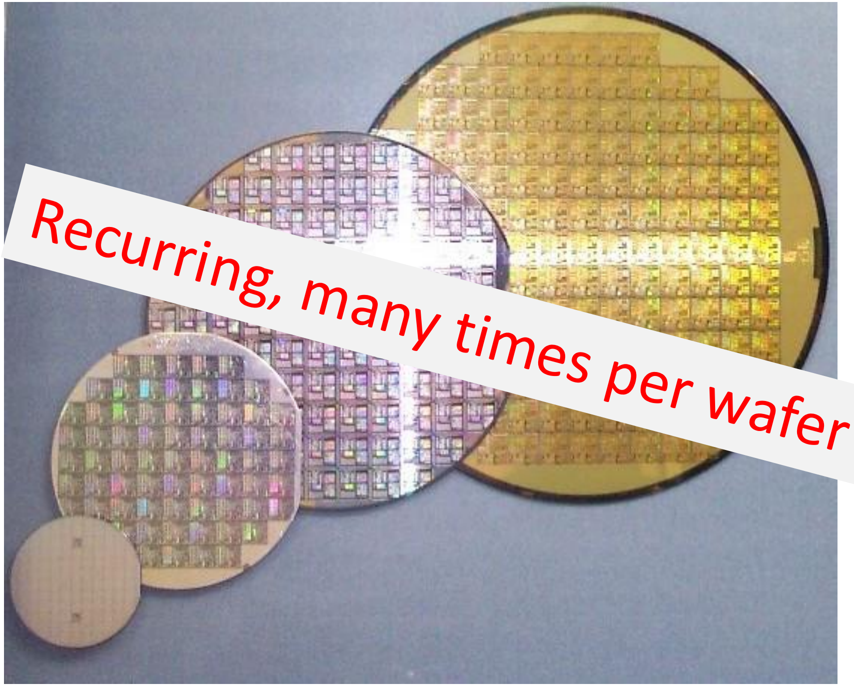
Silicon etch in KOH

Advanced microelectronics need up to 20 litho or more steps

Thin film deposition
Oxidation, CVD, PVD, …



Patterning of thin film
Create structures



Recurring, many times per wafer

Print resolution (document, photos,...)

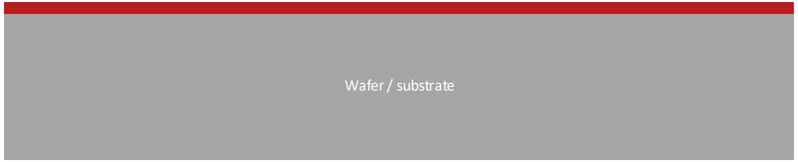
DPI (dot/in)	dpcm (dot/cm)	Pitch (µm)
300	118	85
2540	1000	10
4000	1575	6

→ Need much improved resolution to reach micron, sub-micron, 10nm transistors

Yellow room (UV-sensitive photoresist)

Lithography process flow

- Substrate preparation
- Resist coating and pre-baking
- Resist exposure
- Resist development
- Pattern transfer (etching, lift-off)
- Resist stripping



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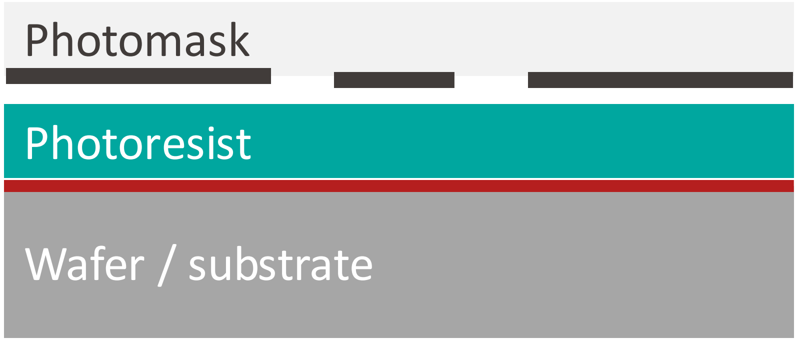

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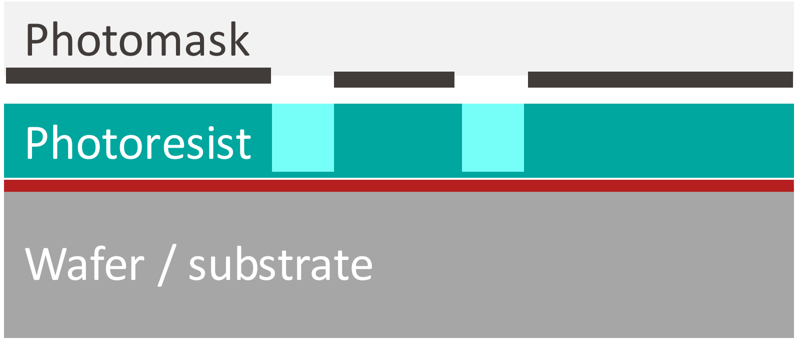

- What is going on in the Photoresist?

Lithography process flow

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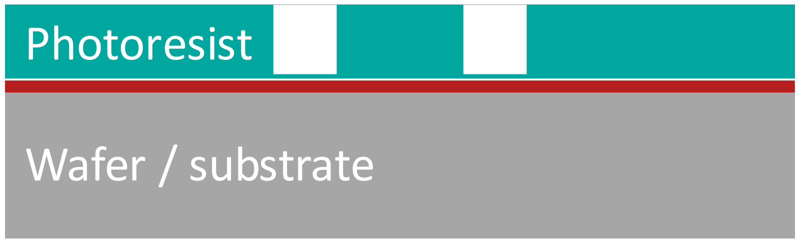
- Resist stripping



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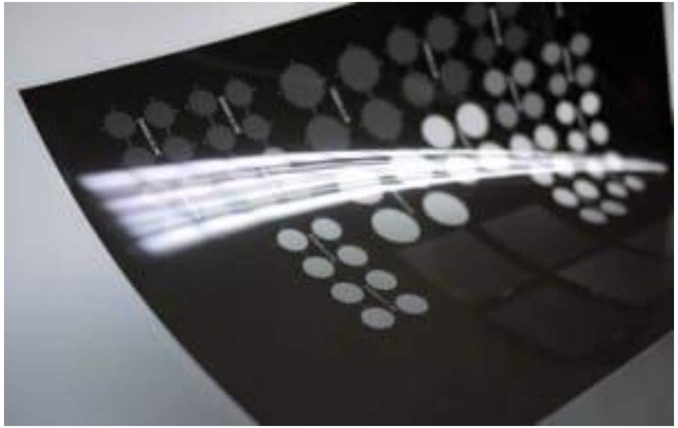
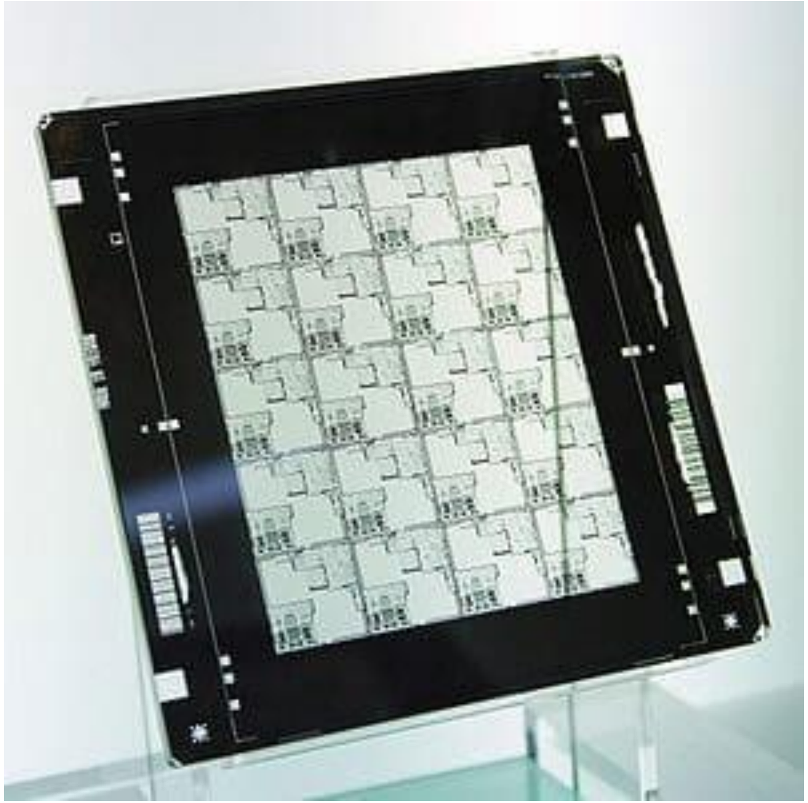
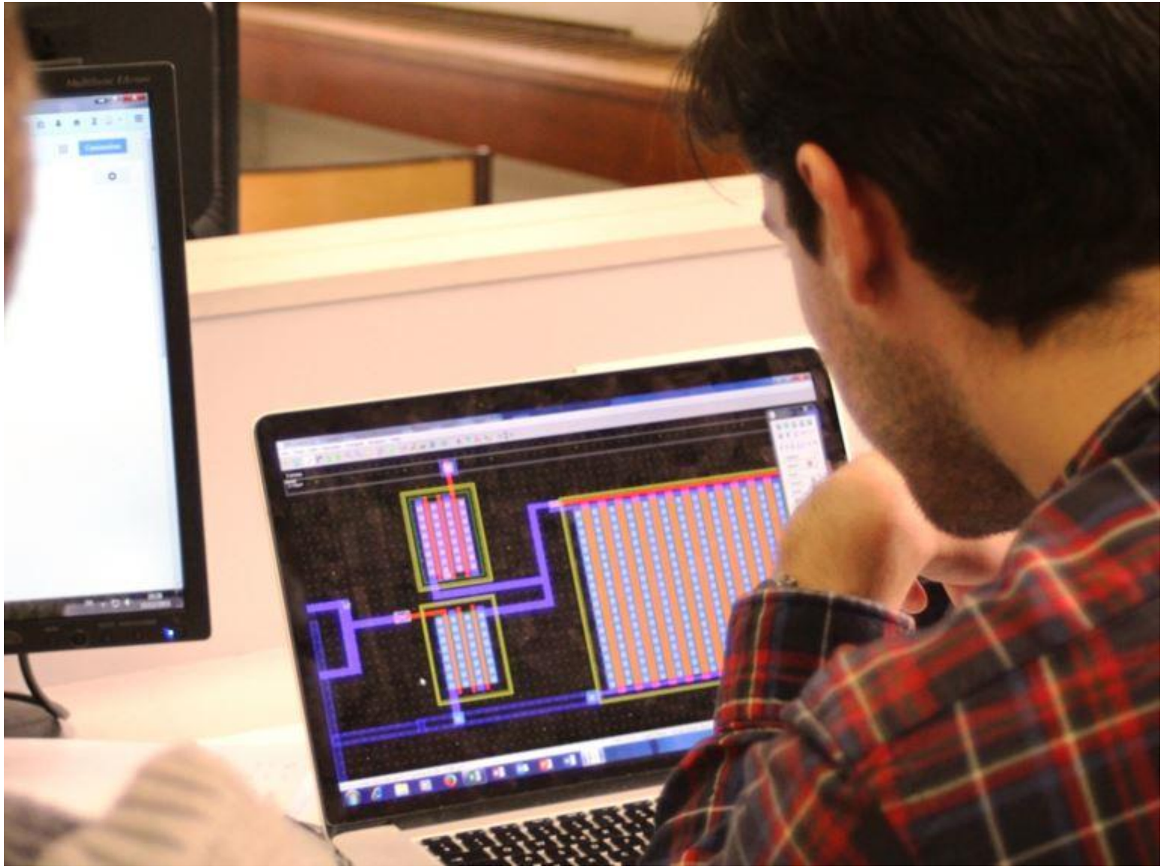
    - microcontact printing
    - scanning nanoprobes

How to make a photo mask?





From design to a micro/nanodevice



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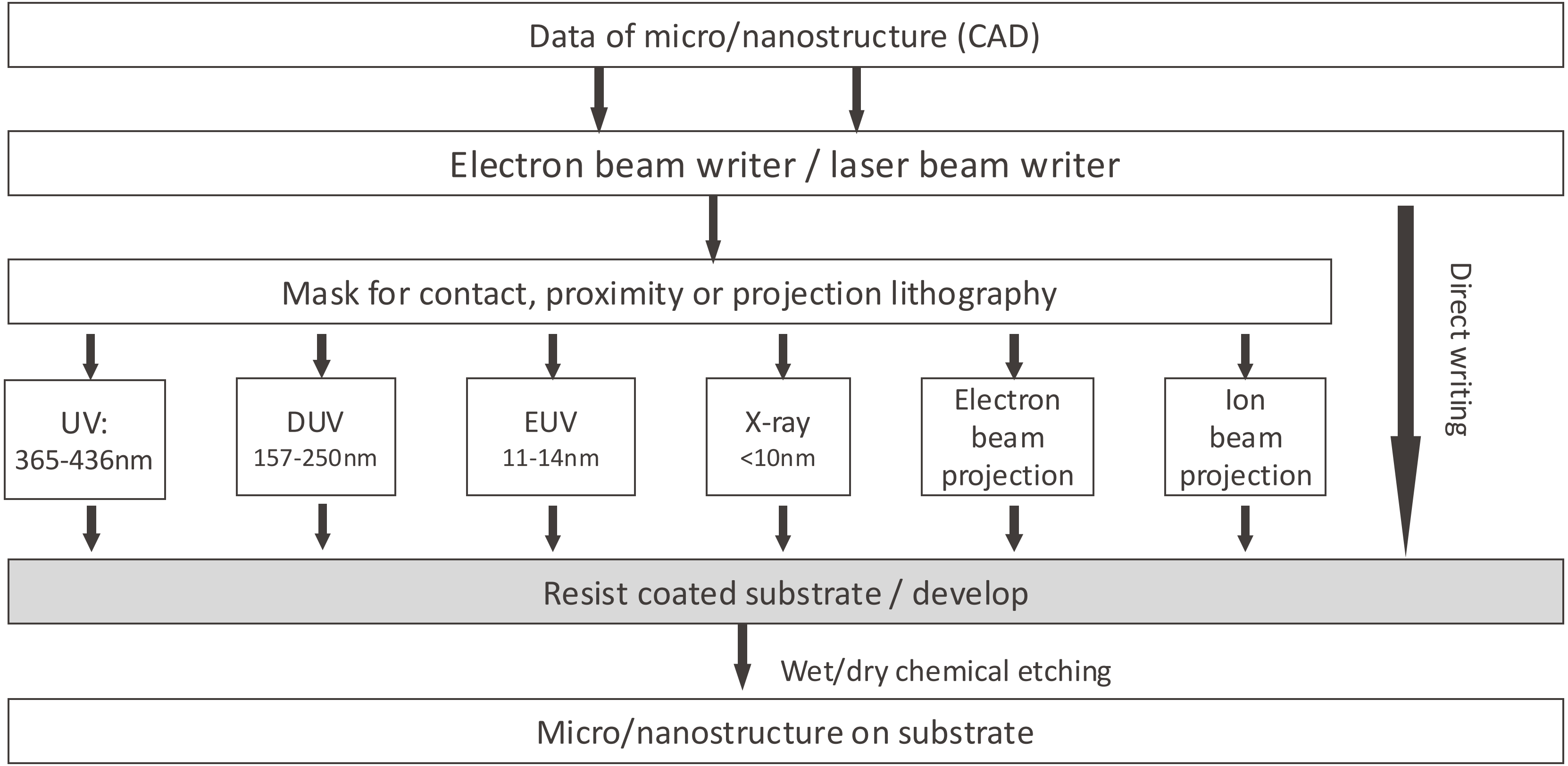
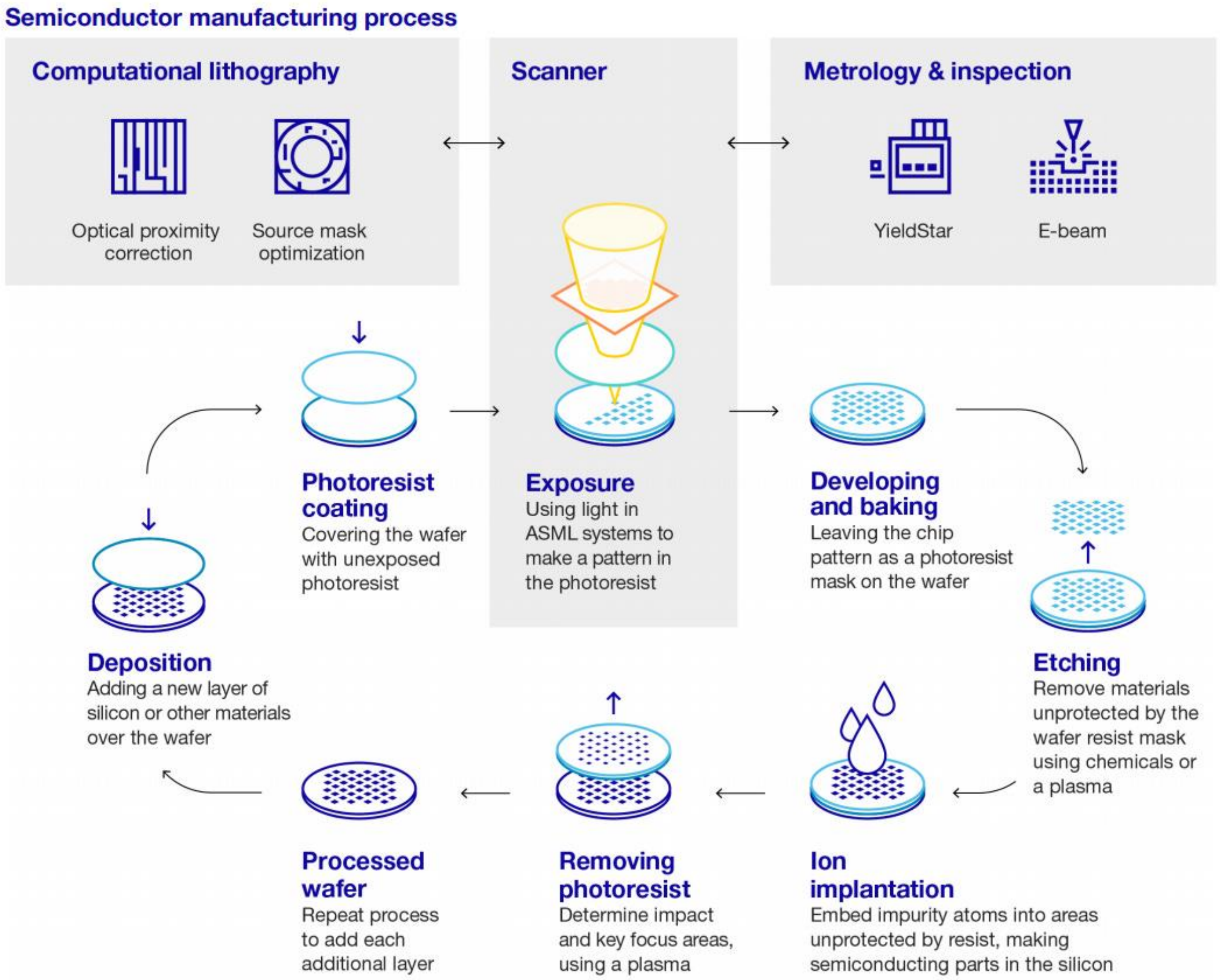
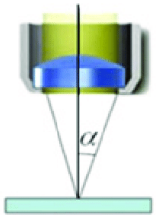




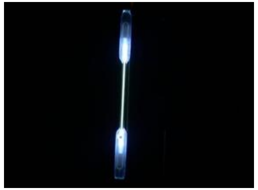
https://www.fabricatedknowledge.com/p/lithographyandasml

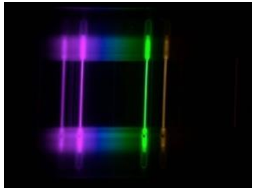
Lithography is limited by diffraction

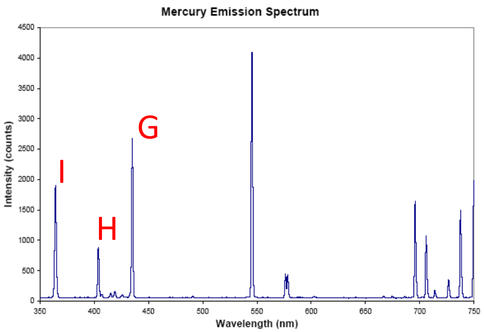
Abbe's Diffraction Limit



$$\Delta x \cong \frac{\lambda}{2n\sin\alpha}$$







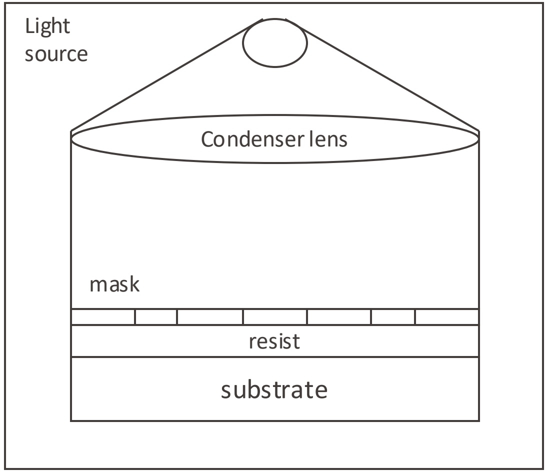
Wavelength [nm]	Source	Range
436	Hg arc lamp	G-line
405	Hg arc lamp	H-line
365	Hg arc lamp	I-line
248	Hg/Xe arc lamp, KrF excimer laser	Deep UV (DUV)
193	ArF excimer laser	DUV
157	F2 laser	Vacuum UV (VUV)
~ 10	Laser-produces plasma sources	Extreme UV (EUV)
~ 1	X-ray tube, syncrotonon	X-Ray

Contact and proximity

- Contact exposure:
  - Mask is in physical contact with substrate
  - Best resolution (diffraction limited)
  - Risk of contamination

- Proximity exposure:
  - Mask is a few micrometers above the substrate
  - Loss in resolution
  - No risk of contamination

contact

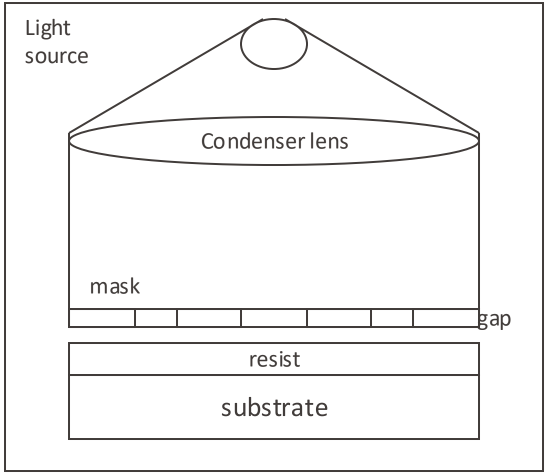


$$MFS = \sqrt{d \times \lambda}$$

$$d = thickness(resist)$$

$$\lambda = wavelength$$

proximity



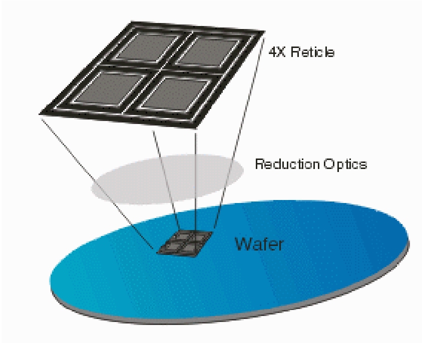
$$MFS \approx \sqrt{(d + g) \times \lambda}$$

$$d = thickness(resist)$$

$$g = gap$$

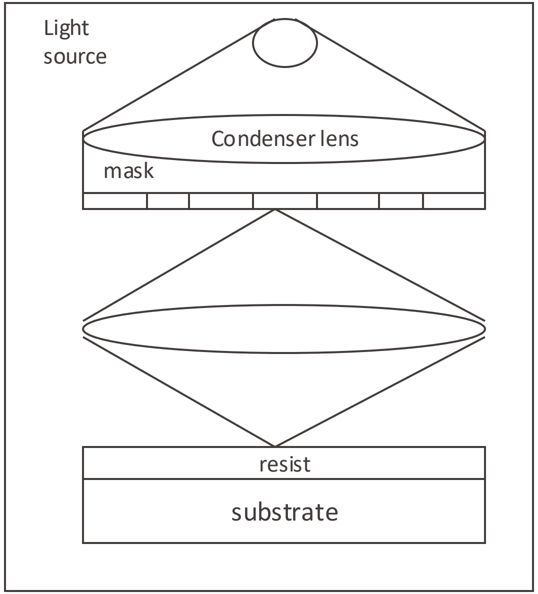
$$\lambda = wavelength$$

Projection lithography (DUV stepper)



- Mainly used today for IC industry
- Picture of the mask is projected
- No contact
- No deterioration
- Excellent resolution (reduction e.g. 4x, 5x)
- Reduction of errors
- Stepper, x-y movement, from field to field

projection



Rayleigh criterion says:
MFS=0.61*λ/NA

In microlithography:
MFS=k_1*λ/NA
k_1=technology cte (0.5-0.9)
Non-ideal behavior of equipment
Lens error
Resist processing, shape, etc.

$$MFS = \sqrt{d \cdot \lambda}$$

$$d = thickness(resist)$$

$$\lambda = wavelength$$

Resolution enhancement of Optical Lithography

- Resolution R: $$R = k_1 \frac{\lambda}{NA}$$
- Depth of Focus DOF: $$DOF = k_2 \frac{\lambda}{NA^2}$$

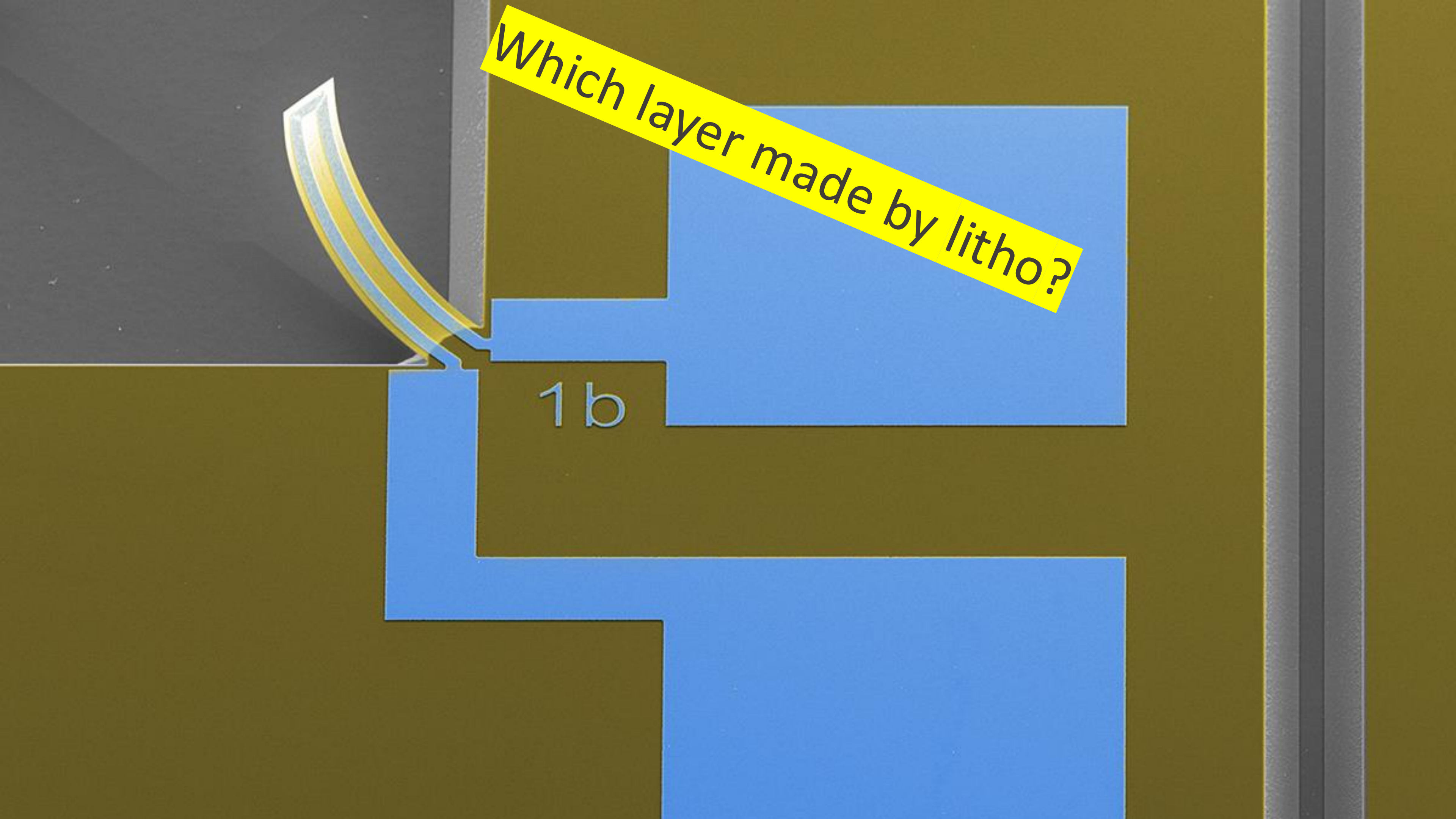
- To decrease R: → need to decrease λ and increase NA (stepper)
- But: DOF decreases too

- → need to decrease k_1
- k_1 = optical engineering = f(resist, mask , illumination)

- Examples: Optical Proximity correction (OPC), Phase shift mask (PSM), Off-axis illumination (OAI)

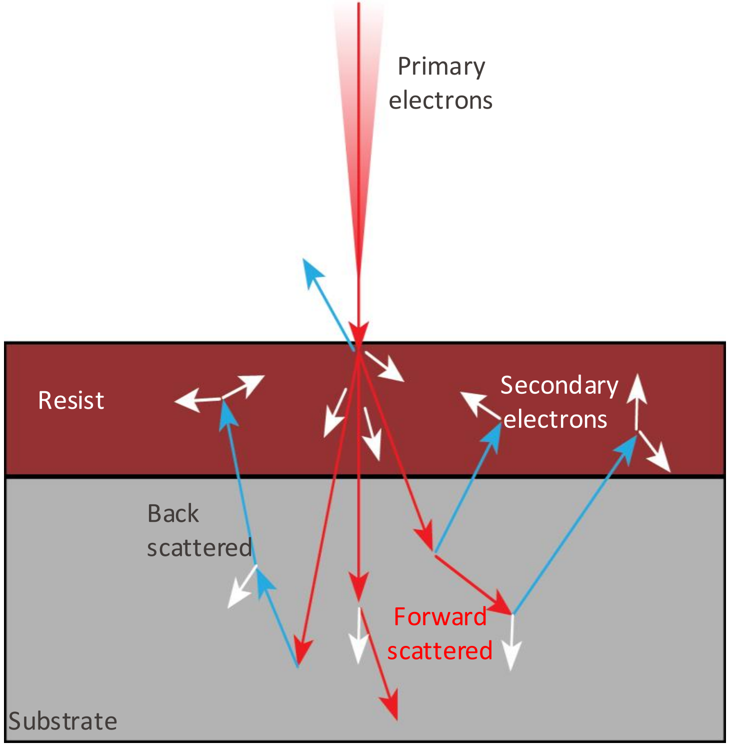
2 possible ways to make metal wires

- Deposition of metal + lithography + etching
- Lithography + deposition of metal + resist stripping **(lift-off)**


Which layer made by litho?
1b

How to break the diffraction limit?

- Use Electron-beam lithography
  - No photons but electrons
  - Primary electrons hit the sample
  - Forward scattered
  - Travel through the resist with high energy
  - Some electrons are back-scattered
  - Responsible for the broadening of resist exposure



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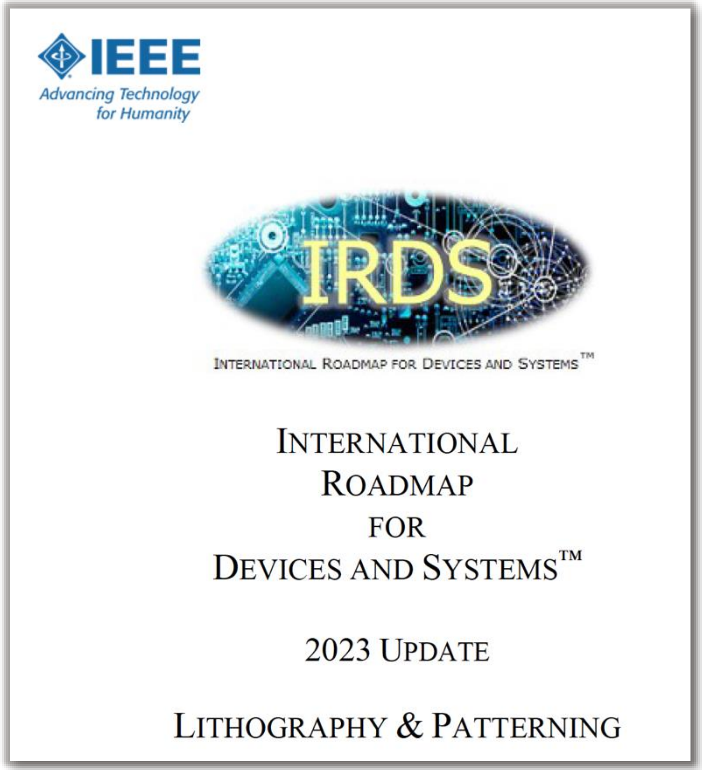

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2023 UPDATE

LITHOGRAPHY & PATTERNING

Table LITH-1 *Lithography Technology Requirements*

Parameter	2022	2025	2028	2031	2034	2037
MPU / Logic						
Logic device technology naming [F}	G48M24	G45M20	G42M16	G40M16T2	G38M16T4	G38M16T6
Logic Industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Logic device structure options	FinFETLGAA	LGAA	LGAA	LGAA-3D	LGAA-3D	LGAA-3D
MPU/ASIC Minimum Metal ½ pitch (nm)	12.0	10.0	8.0	8.0	8.0	8.0
Metal LWR (nm) [C]	1.8	1.5	1.2	1.2	1.2	1.2
Metal CD control (3 sigma) (nm) [B]	1.8	1.5	1.2	1.2	1.2	1.2
Contacted poly half pitch (nm)	24.0	22.5	21.0	20.0	19.0	19.0
Physical Gate Length for HP Logic (nm)	16.0	14.0	12.0	12.0	12.0	12.0
Gate LER (nm) [C]	1.1	1.0	0.8	0.8	0.8	0.8
Gate CD control (3 sigma) (nm) [B]	1.6	1.4	1.2	1.2	1.2	1.2
Overlay (3 sigma) (nm) [A}	2.4	2.0	1.6	1.6	1.6	1.6
Metal CDU (nm)	1.8	1.5	1.2	1.2	1.2	1.2
Metal LER (nm)	1.3	1.1	0.8	0.8	0.8	0.8
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	12.0					
FinFET Fin width (nm)	5.0					
Fin CD control (3 sigma) (nm) [B]	0.5					
FIN LER (nm) [C]	0.35					
Lateral Gate All Around (LGAA) pitch		26.00	24.00	24.00	23.00	23.00
LGAA minimum width		7.0	6.0	6.0	6.0	6.0
LGAA CD control (3 sigma) (nm) [B]		0.7	0.6	0.6	0.6	0.6
GAA LwR (nm) [C]		0.7	0.6	0.6	0.6	0.6
MPU/ASIC minimum contact hole pitch (nm)	48	45	42	40	38	38
MPU/ASIC minimum contact hole CD (nm)	24	23	21	20	19	19
MPU/ASIC Via pitch	34	28	23	23	23	23
MPU/ASIC Via half pitch	17	14	11	11	11	11
MPU/ASIC minimum contact hole or via CDU (nm)	2.55	2.12	1.70	1.70	1.70	1.70
DRAM						
Dram Minimum 1/2 pitch (nm)	17	14	11	8.4	7.7	7.0
CD control (3 sigma) (nm) [B]	1.7	1.4	1.1	0.8	0.8	0.7
Mininum contact/via after etch (nm) [D]	17	14	11	8.4	7.7	7.0
Minimum contact/via pitch(nm)[D]	51	42	33	25	23	21
Overlay (3 sigma) (nm) [A]	3.4	2.8	2.2	1.7	1.5	1.4

Today - Lithography

https://www.asml.com/en/technology/lithography-principles

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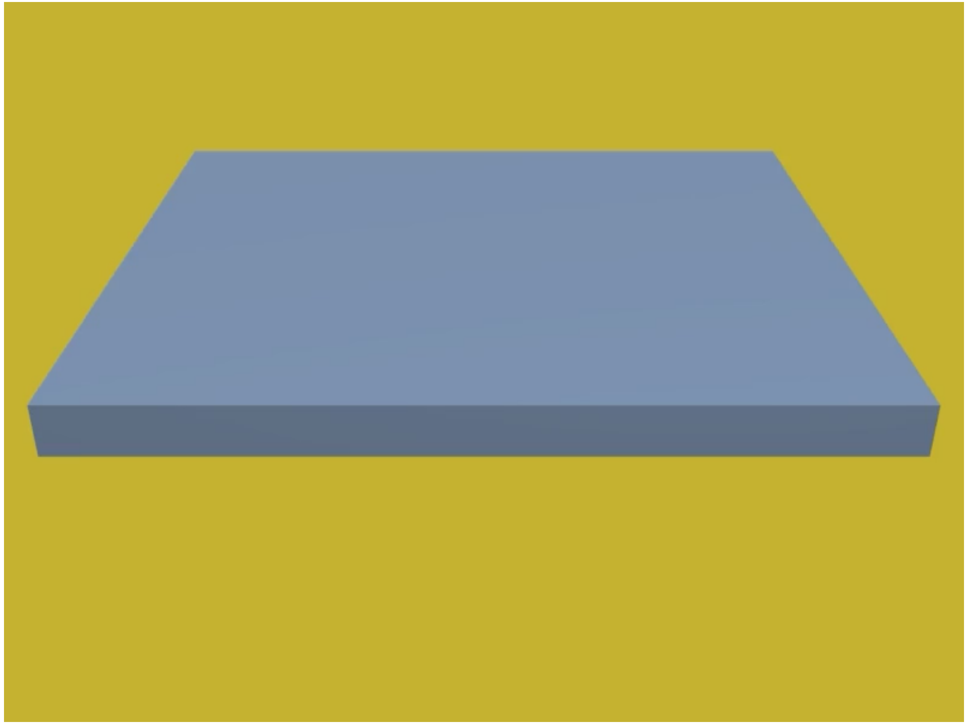
Stencil lithography (cartoon)



- Patterning without photoresist
- Very small (<100nm)
- Very large (mm)
- Vacuum clean

- Deposition
- Etching
- Implantation

Stencil fabrication

LPCVD 50-500 nm thick SiN

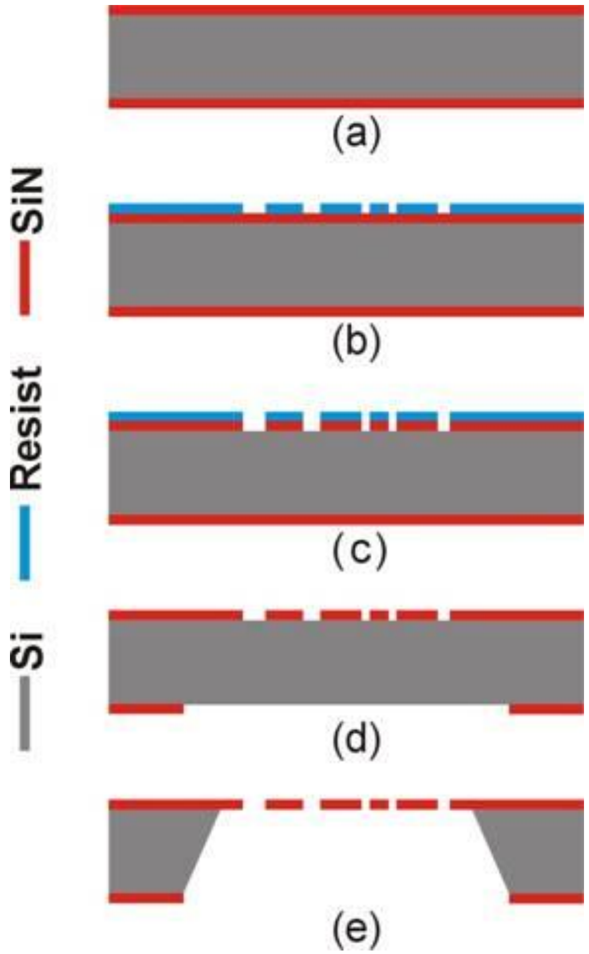
Pattern definition in photoresist

Pattern transfer into SiN

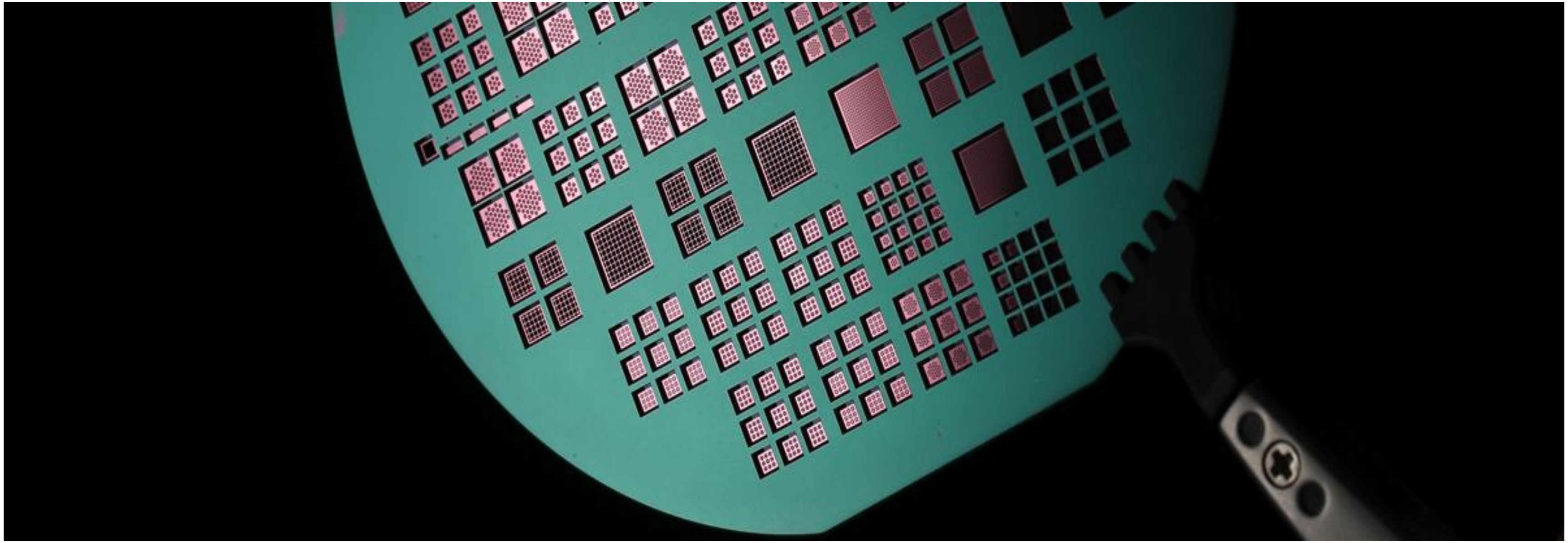
Membrane window definition and KOH etching

Fabrication of nanoscale apertures in membrane by:

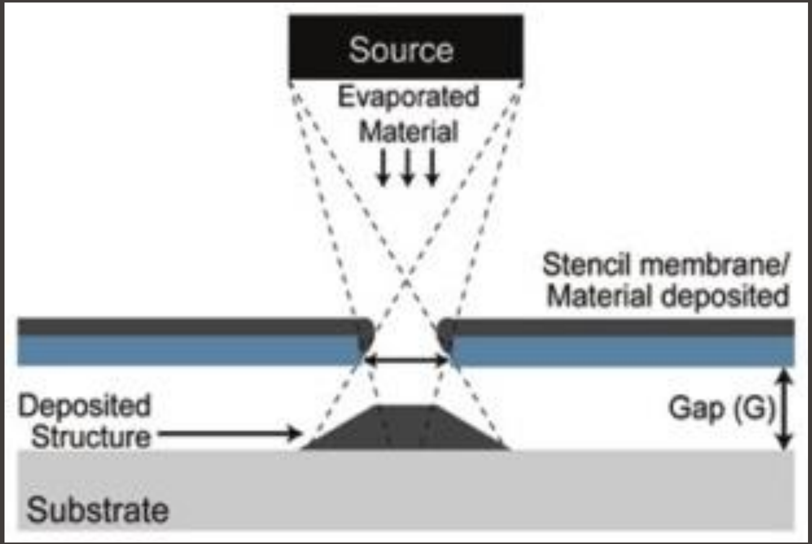
- Focused Ion Beam Milling
- Electron beam lithography
- Laser interference lithography
- Nanoimprint lithography
- Deep UV lithography



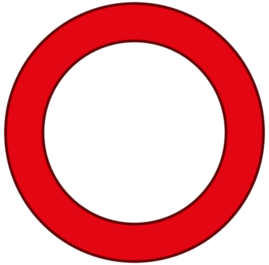
Nanostencil

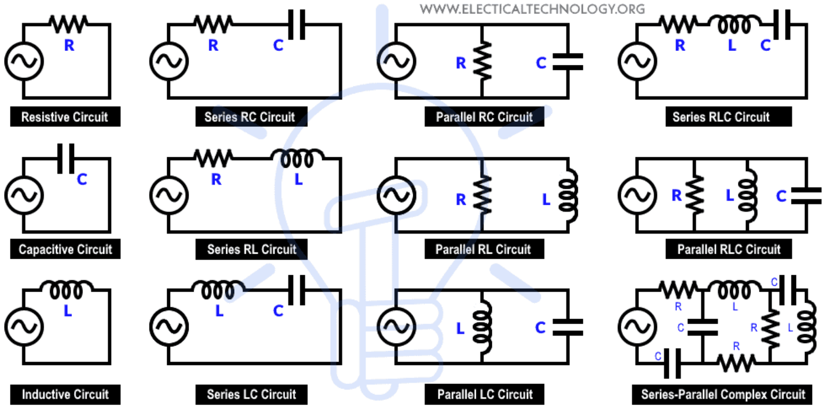


What are the challenges? What are the opportunities?

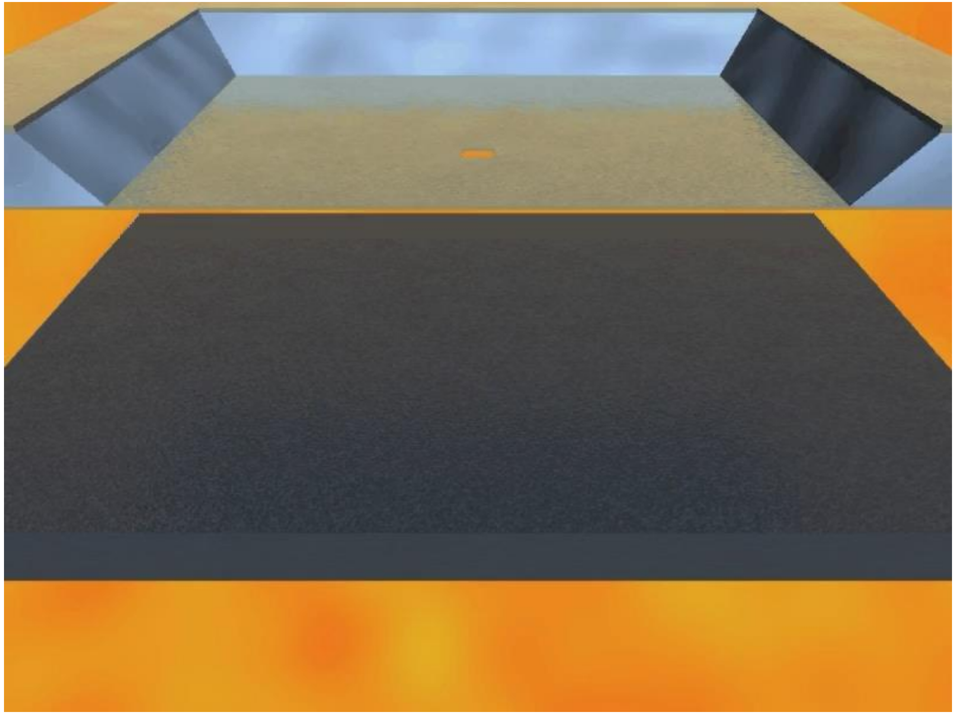


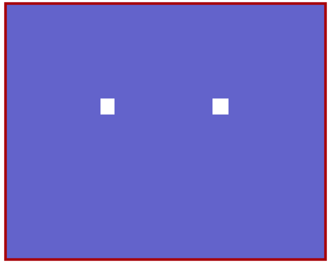
How to do closed topology?



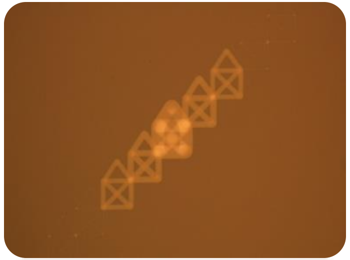


Dynamic stenciling

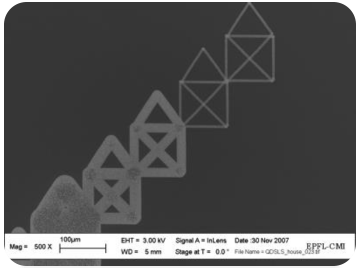




stencil



Free motion



SEM image

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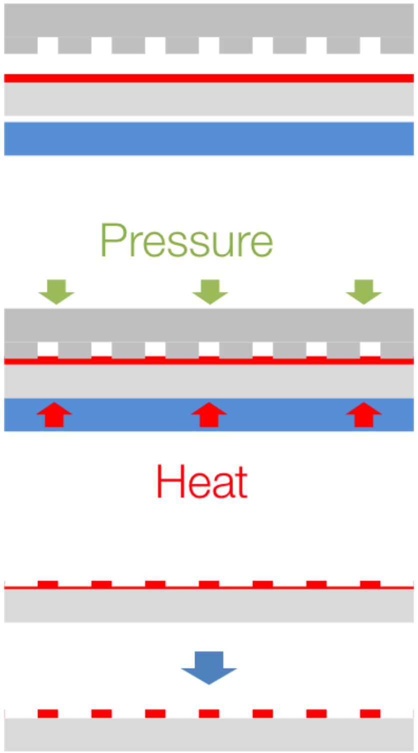
Nano-Imprint Lithography



Imprint stack preparation

Stamp (or mold), Resist, Substrate, Chuck

Imprinting

Pressure / temperature / time profile

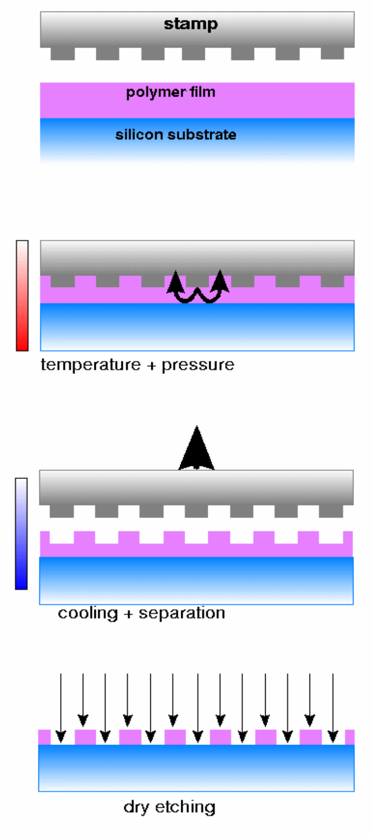
Separation

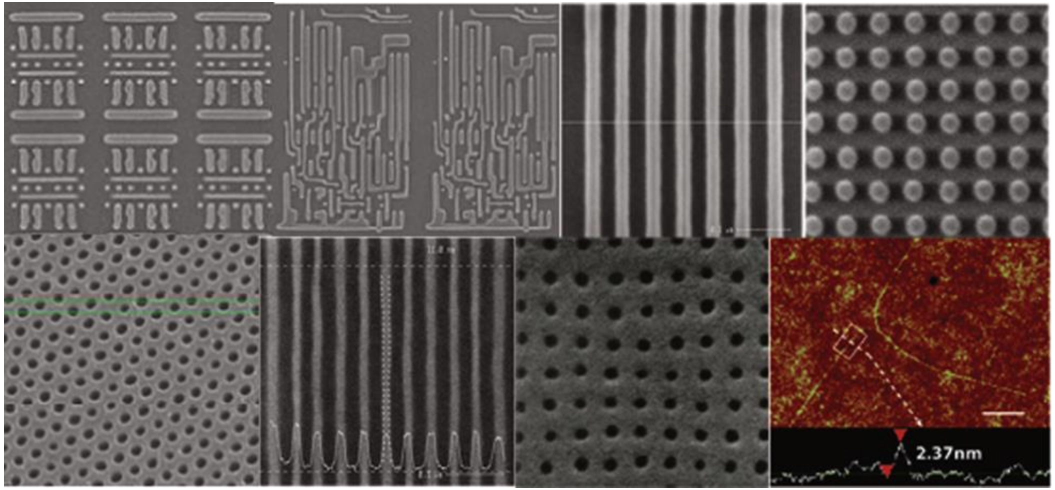
Temp control

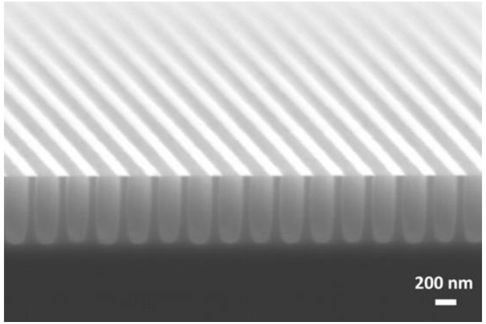
Residual layer etch

Remove thin resist layer by O2 plasma

Nano-Imprint Lithography

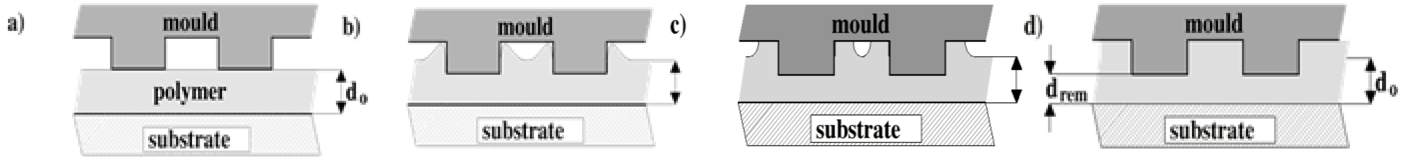


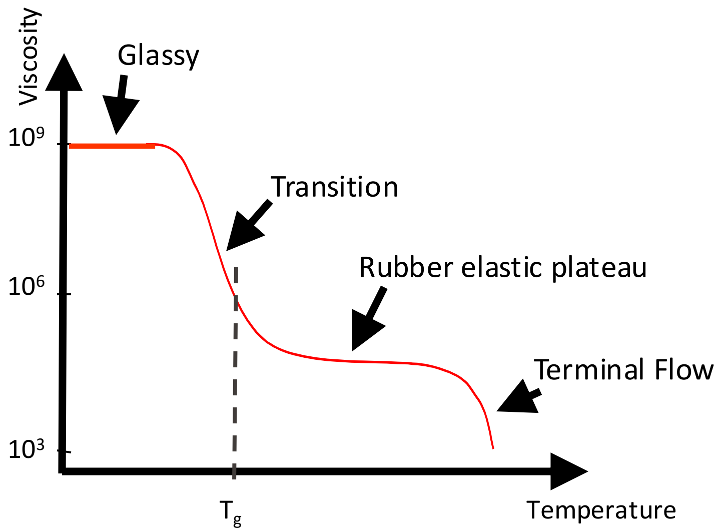


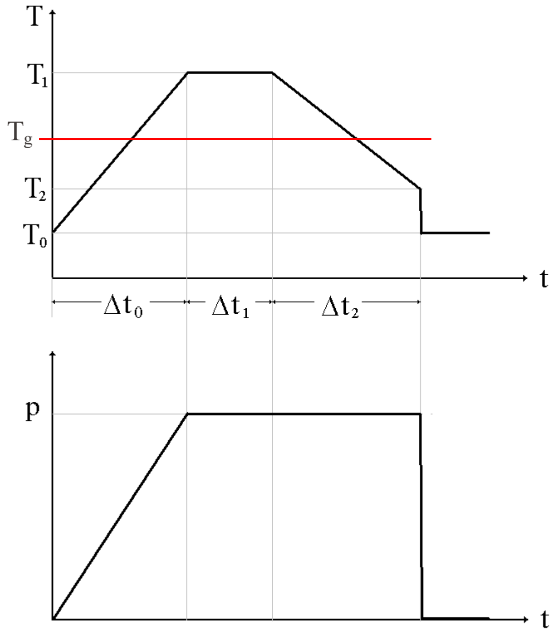


S. Chou et al. *Science 5 April 1996: Vol. 272 no. 5258 pp. 85-87*

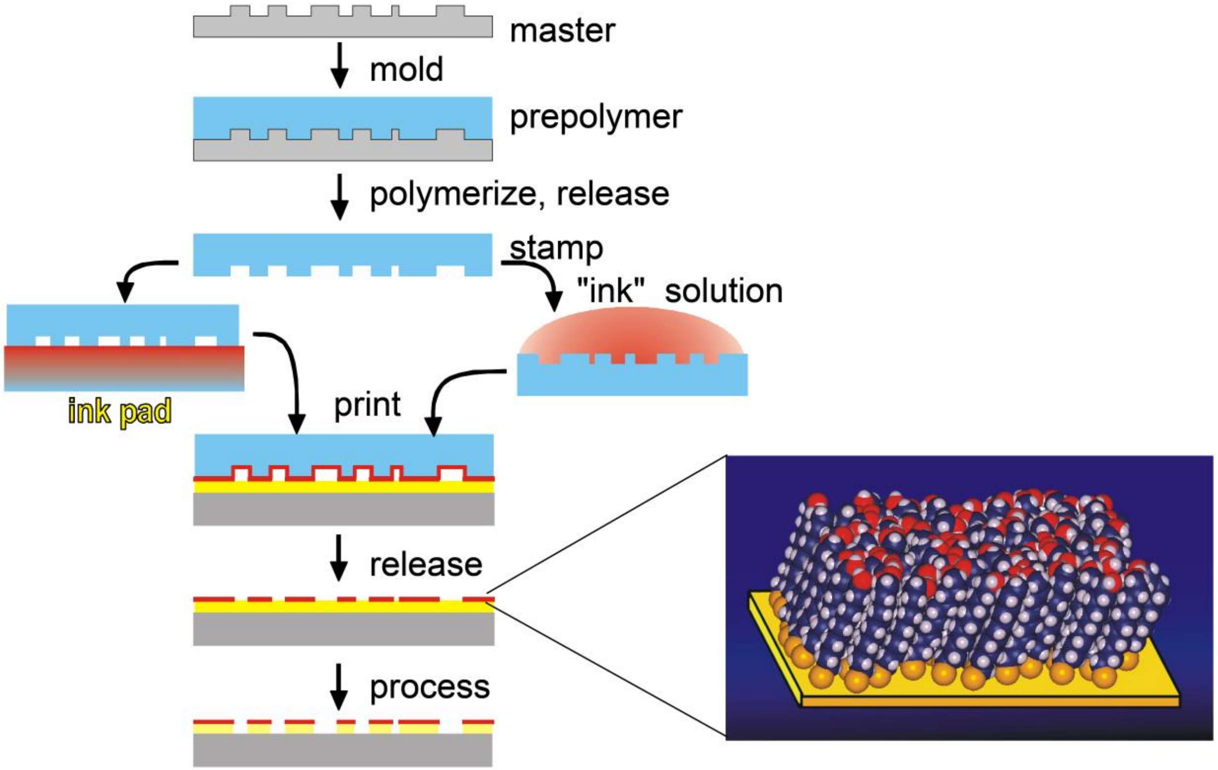
Nanoimprint Process Model







Microcontact Printing (µCP)



http://zurich.ibm.com

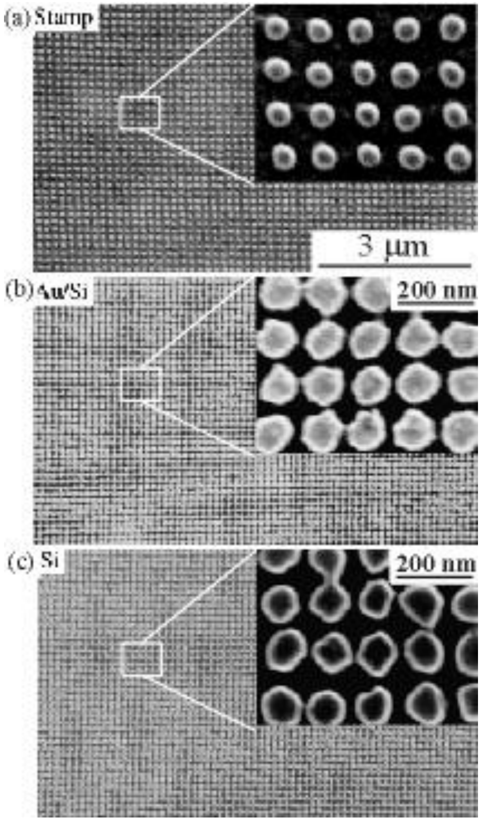
Microcontact Printing

High-resolution µCP:

a) Scanning electron micrograph of a stamp with 60 nm dots.

b) The corresponding gold dots fabricated by printing and etching were slightly broadened due to ink diffusion and substrate roughness.

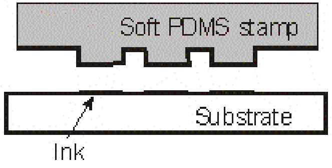
c) The gold pattern served as a mask to etch the bare regions 250 nm deep into the underlying silicon by reactive ion etching.

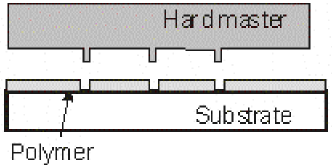


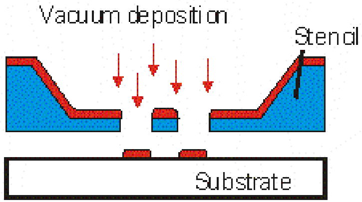
http://zurich.ibm.com

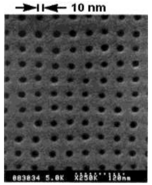
Emerging Nanopatterning Methods
(Replication)

Soft-lithography	Nanoimprint lithography	Nanostencil lithography
Ink delivery molecules, wet *soft-contact*	Thermo-mechanical, nano-imprinting, *hard contact*	Local deposition stencil, vacuum *no contact*

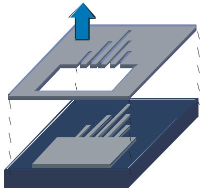








10 nm
Candidate for
Integrated Circuit



Today - Lithography

- Key aspects to remember
  - Resists
  - Writer and projection/mask
  - Resolution and throughput
  - Lift-off
- Industry standard today
- Alternative lithography
  - Stencil
  - Nanoimprint
  - microcontact printing
  - scanning nanoprobes